Amendments to the Specification:

Please replace paragraph **0021** with the following amended paragraph:

[0021] Fig[s]. 2A is a highly enlarged schematic side cross-sectional view of a semiconductor die showing a portion of the cell array and the field termination.

Please insert the following new paragraph after paragraph **0021**:

[0021.1] Fig. 2B is a cross-sectional view of another embodiment of a semiconductor die showing a portion of the cell array and the field termination.

Please replace paragraph **0023** with the following amended paragraph:

[0023] Figs. 4-4[k]K are schematic side cross-sectional views showing the individual steps of the process diagrammed in Fig. 3. The figure numbers for the detailed views in Figs. 4-4[k]K are shown parenthetically under the corresponding diagram boxes in Fig. 3.

Please replace paragraph **0024** with the following amended paragraph:

[0024] Figs. 5, 5A, and 5[b]B are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor.

Please replace paragraph **0025** with the following amended paragraph:

[0025] A cell array 10, including a plurality of rows 12 of trenched DMOS transistors, is shown in Fig. 1. Cell array 10 has an open cell configuration, i.e., trenches 14 run in only one direction, rather than forming a grid. Individual cells are formed by alternating n+ source contacts 16 and p+ contacts 18 in rows 20 that run parallel to and between trenches 14. The configuration of the regions of each row that have an n+ source contact are shown in cross-section in Fig. 1[a]A, while the regions that have a p+ contact are shown in Fig. 1[b]B.

Please replace paragraph **0026** with the following amended paragraph:

[0026] As shown in Figs. 1[a]A and 1[b]B, each trenched DMOS transistor includes a doped n+ substrate (drain) layer 22, a more lightly doped n- epitaxial layer 24, and a gate electrode 28. Gate electrode 28 comprises a conductive polysilicon that fills a trench 14. A gate oxide 26 coats the walls of the trench and underlies the polysilicon. The top surface of the polysilicon is recessed from the surface 30 of the semiconductor substrate by a distance R (typically from about 0 to 0.4 μm). N+ doped source regions 32a, 32b are positioned one on each side of the trench 14. A dielectric layer 35 covers the trench opening and the two source regions 32a, 32b. Extending between the source regions of adjacent cells is a p+ heavy body region 34 and, beneath it, a flat-bottomed p- well 36. In the areas of the cell array which have a n+ contact 16, a shallow n+ doped contact region extends between the n+ source regions. A source metal layer 38 covers the surface of the cell array.

Please replace paragraph **0027** with the following amended paragraph:

[0027] The transistor shown in Figs. 1[a]A and 1[b]B includes several features that enhance the ruggedness of the transistor and its resistance to avalanche breakdown degradation.

Please replace paragraph **0031** with the following amended paragraph:

[0031] Lastly, referring to Fig. 2, the cell array is surrounded by a field termination junction 40 which increases the breakdown voltage of the device and thaws avalanche current away from the cell array to the periphery of the die. Field termination junction 40 is a deep p+ well, preferably from about 1 to 3 μm deep at its deepest point, that is deeper than the p+ heavy body regions 34 in order to reduce the electric field caused by the junction curvature. A preferred process for making the above-described transistors is shown as a flow diagram in Fig. 3, and the individual steps are shown schematically in Figs. 4-4[k]K. It is noted that some steps that are conventional or do not require illustration are described below but not shown in Figs. 4-4[k]K. As indicated by the arrows in Fig. 3, and as will be discussed below, the order of the steps shown in Figs. 4-4[k]K can be varied. Moreover, some of the steps shown in Figs. 4-4[k]K are optional, as will be discussed.

Please replace paragraph **0033** with the following amended paragraph:

[0033] Next, the field termination junction 40 is formed by the steps shown in Figs. 4-4[c]C. In Fig. 4, an oxide layer is formed on the surface of the epitaxial layer. Preferably, the thickness of the oxide is from about 5 to 10 kÅ. Next, as shown in Fig. 4[a]A, the oxide layer is patterned and etched to define a mask, and the p+ dopant is introduced to form the deep p+ well field termination. A suitable dopant is boron, implanted at an energy of from about 40 to 100 keV and a dose of 1E14 ($1x10^{14}$) to 1E16 cm^{-2}. As shown in Fig. 4[b]B, the p+ dopant is then driven further into the substrate, *e.g.*, by diffusion, and a field oxide layer is formed over the p+ junction. Preferably the oxide thickness is from about 4 to 10 kÅ. Finally, the oxide (Fig. 4) over the active area of the substrate (the area where the cell array will be formed) is patterned and removed by any suitable etching process, leaving only the field oxide in suitable areas. This leaves the substrate ready for the following steps that will form the cell array.

Please replace paragraph **0034** with the following amended paragraph:

[0034] It is noted that, as an alternative to steps 4-4[c]C, a suitable field termination structure can be formed using a ring-shaped trench which surrounds the periphery of the cell array and

acts to lessen the electric field and increase the resistance to avalanche breakdown degradation. This trench field termination does not require a field oxide or deep p+ body junction to be effective. Consequently, it can be used to reduce the number of process steps. Using a trench ring (or multiple concentric trench rings) to form a field termination is described in, *e.g.*, U.S. Patent No. 5,430,324, the full disclosure of which is hereby incorporated herein by reference. Preferably, the trench would have substantially the same depth as the trenches in the cell array. An exemplary embodiment for a trench termination structure is shown in Figure 2B. Termination trenches 40T form concentric rings around the edge of the device. Termination trenches 40T can be filled with either floating conductive material such as polysilicon or floating dielectric material such as silicon dioxide. Also, the p-type well regions on either sides of termination trenches 40T can be made either shallower than the trenches or deeper than the trenches.

Please replace paragraph **0035** with the following amended paragraph:

[0035] The cell array is formed by the steps shown in Figs. 4[d]D-4[k]K. First, a plurality of trenches are patterned and etched into the epitaxial layer of the substrate (Fig. 4[d]D). Preferably, as noted above, the trenches are formed using the process described in U.S. Application No. 08/959,197, filed on October 28, 1997, now U.S. Patent No. 6,103,635, so that the upper and lower corners of each trench will be smoothly rounded. As shown in Fig. 1 and described above, the trenches are patterned to run in only one direction, defined as an open cell structure. After trench formation, a gate oxide layer is formed on the trench walls, as is well known in the semiconductor field. Preferably the gate oxide has a thickness of from about 100 to 800 Å.

Please replace paragraph **0036** with the following amended paragraph:

[0036] Next, as shown in Fig. 4[e]E, polysilicon is deposited to fill the trench and cover the surface of the substrate, generally to a thickness of from about 1 to 2 μm depending on the trench width (shown by the dotted lines in Fig. 4[e]E). This layer is then planarized by the nature of its thickness relative to the trench width, typically from about 2 to 5 k Å (indicated by solid lines in

Fig. 4[e]E). The polysilicon is then doped to n-type, *e.g.*, by conventional $POCL_3$ doping or by phosphorus implant. The backside of the wafer need not be stripped (as is conventionally done prior to doping the polysilicon to enhance defect gettering) because any further doping of the highly doped substrate would be unlikely to result in any enhancement in defect gettering.

Please replace paragraph **0037** with the following amended paragraph:

[0037] The polysilicon is then patterned with a photoresist mask and etched to remove it from the trench areas, as shown in Fig. 4[f]F. A small recess between the top of the polysilicon in the trench and the substrate surface inherently results when the polysilicon is etched completely to remove all of the polysilicon from the substrate surface. The depth of this recess must be controlled so that it does not exceed the depth of the n+ source junction that will be formed in a later step. To reduce the need to carefully control this aspect of the process, a relatively deep n+ source junction is formed, as will be discussed below.

Please replace paragraph **0038** with the following amended paragraph:

[0038] Then, as shown in Fig. 4[g]G, the p- well is formed by implanting the dopant, *e.g.*, a boron implant at an energy of 30 to 100 keV and a dosage of 1E13 to 1E15, and driving it in to a depth of from about 1 to 3 μm using conventional drive in techniques.

Please replace paragraph **0040** with the following amended paragraph:

[0040] First, a mask is formed over the areas that will not be doped to p+, as shown in Fig. 4[h]H. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see Fig. 4[k]K, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p- well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (*e.g.*, boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of 1E15 to 5E15 cm^{-2}, and a second boron implant at an energy of 20 to 40 keV and a dose of 1E14 to 1E15 cm^{-2}. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that

it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact 18. The resulting p+ heavy body junction is preferably about 0.4 to 1 μm deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5 μm deep), and includes a region of high dopant concentration near the interface with the p-well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in Fig. 5.

Please replace paragraph **0042** with the following amended paragraph:

[0042] After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts 18 (Figs. 1 and 1[b]B), as shown in Fig. 4[i]I. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A-A and B-B and cross-sectional views A-A and B-B in Fig. 4I, which correspond to Figs. 1[a]A and 1[b]B).

Please replace paragraph **0043** with the following amended paragraph:

[0043] The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of 5E15 to 1E16 cm^{-2} followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of 1E15 to 5E15 cm^{-2}. The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8 μm after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts 16 (see Figs. 1 and 1[a]A) by compensating (converting) the p-type surface of the p+ heavy body to n-type in the desired contact area. The

preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in Figs. 5[a]A and 5[b]B, respectively.

Please replace paragraph **0046** with the following amended paragraph:

[0046] A dielectric material, *e.g.*, borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (Fig. 4J), after which the dielectric is patterned and etched (Fig. 4[k]K) to define electrical contact openings over the n+ and p+ contacts 16, 18.